Technical Description

for the

OPTRA

Risley Prism Assembly (RPA) Controller

Prepared for:

Customer Information

Prepared by:

OPTRA, Inc
461 Boston Street
Topsfield, MA 01983
(978)-887-6600

Rev. -

Date: 11/10/09

This page is intentionally left blank!

(Back of Cover Page)

Revision Summary

Rev	Date	Description
-	11/05/2009	Initial Release Based on the RPSA ICD 3-0352-0. Changes from that include: ▪ Renamed document ▪ Removed references to internal interfaces ▪ Updated Command Port's baud rate to 57600 bps

This page is intentionally left blank!
(Back of Revision Page)

Table Of Contents

List Of Figures

List Of Tables

1.0 OVERVIEW

Figure 1-1 illustrates how a pair of prisms can be used to steer a laser beam. The angle off axis (ALT) is given by the relative rotational angle between the two prisms, and the direction by the rotational angle (ϕ) of the prism pair. For prism pairs of similar geometry, the deviation angle will double when they are in alignment and will cancel when they are in opposition. Accurate rotational positioning of an individual prism is accomplished using a motor and angular position feedback in a closed loop servo control system. The (ALT,ϕ) angle pair is converted into a pair of prism rotation angles (ϕ_{in}, ϕ_{out}), and the controllers actuate the prism motors to null out the error signal between the commanded rotation angles and the actual prism angles as read by the angle encoders. The amount of power is quite reduced in comparison to standard gimbaled systems since the rotating parts are tightly constrained about the rotating axis, resulting in much smaller motor torques.

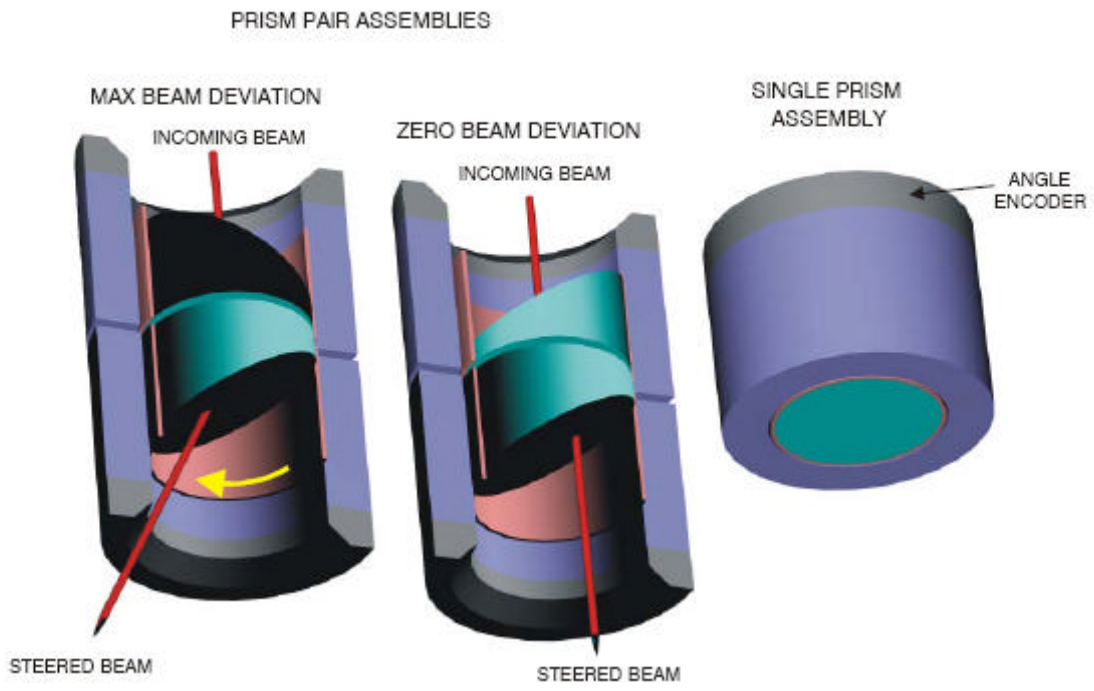

Figure 1-1 Risley prism beamsteering overview

OPTRA's RPA unit accepts and accomplishes formatted beam position and scanning commands. The system design is based on rotating the optical elements in a prism-pair assembly to steer the beam over a wide field of coverage as detailed in Figure 1-2. The advantages of this design are compactness, low susceptibility to vibration, high reliability, and low-costing components.

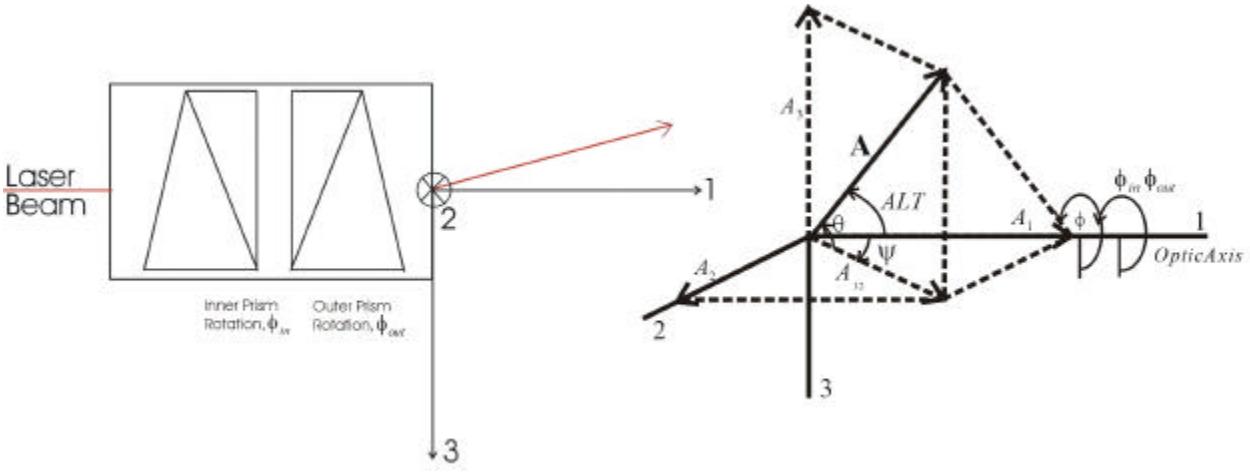

Figure 1-2 RPA system coordinate frame and angle definitions

2.0 TECHNICAL DESCRIPTION

Figure 2-1 shows a detailed view of the RPA processing architecture detailing the various interfaces internal and external to the RPA. The RPA is comprised of three subsystems: the RPA Controller assembly, the RP-xx Risley Prism assembly (for example: an RP-25), and an interconnecting cable. Section 2.0 describes each interface. Section 3.0 details the RP Controller board's connectors and jumpers. Section 4.0 describes the mechanical layout of the RP Controller board.

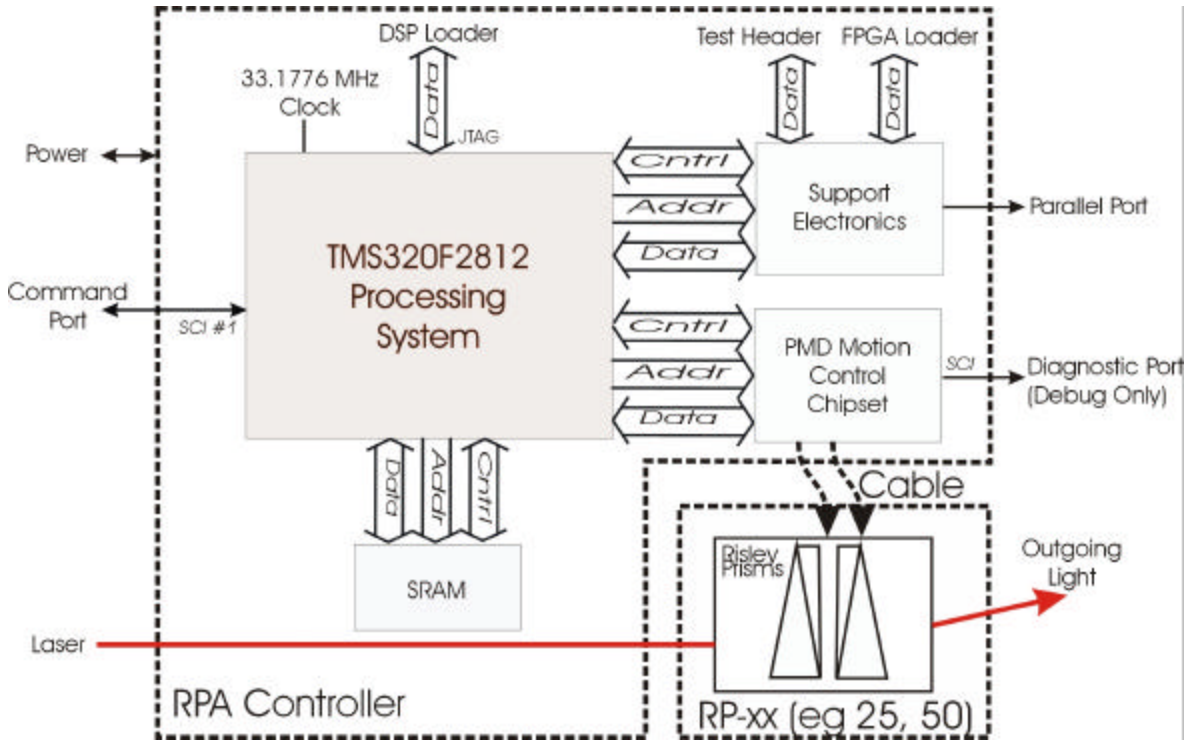

Figure 2-1 RPA Functional Processing Architecture

2.1 Interfaces

2.1.1 Command Port

The Command Port is responsible for accepting formatted command messages from the user and in response, providing status back to the user in the form of formatted status messages. The details of this interface are described in Table 2-1 and Table 2-2. Table 2-3 defines the format of each RPA command message. Table 2-4 defines the format of each RPA response message. This implementation of this port is a portion of Connector JP3 (see section 3.0).

Table 2-1 Command Port Interface Details

Protocol :		LVCMOS or RS232 (Jumper selectable via jumper J1 – See section 3.0)				
Rate :		Messages sent asynchronously as commanded by the user.				
Name	**Description**	**Source**	**Dest.**	**Addr Offset**	**Units**	**Limit/Range**
User_Command_Status	Control and status messages to/from the RPA	User/RPA	RPA/User	N/A	N/A	See Table 2-3 and Table 2-4

Table 2-2 Command Port Serial Messaging Protocol

Start Bit	Data Bit 0	Data Bit 1	…	Data Bit 7	Even Parity Bit	Stop Bit
Baud Rate = 57600 bps						

Table 2-3 RPA Command Message Format

Byte #	**Description**					
0	Message Header Byte (0xCB)					
1	RPA System Mode Command: (0x0 – 0x4, 0xC-0xF)					
	0x00 = Perform RPA Initialization then configure parallel output[1]	0x1 = Command RPA using [Ψ, θ] system pointing angle[2]	0x2 = Command RPA using [ALT, ϕ] system pointing angle[3]	0x3 = Command RPA using [V_{in}, V_{out}] prism velocities[4]	0x4 = Command RPA using [ϕ_{In}, ϕ_{Out}] motor angular positions[5]	0xC–0xF = Customized [w1, w2] system status response C= [Ψ, θ] D= [ALT, ϕ] E=[V_{in},V_{out}] F= [ϕ_{In}, ϕ_{Out}]
2	Parallel Port Mode: 0= [Ψ, θ] 1= [ALT, ϕ] 2= [ϕ_{In}, ϕ_{Out}]	Ψ position command MSByte	ALT position command MSByte	V_{in} inner prism velocity command MSByte	ϕ_{In} inner motor direct command MSByte	Not used
3	Parallel Output Rate (bits 23-16)	Ψ position command LSByte	ALT position command LSByte	V_{in} inner prism velocity command LSByte	ϕ_{In} inner motor direct command LSByte	Not used
4	Parallel Output Rate (bits 15-8)	θ position command MSByte	ϕ position command MSByte	V_{out} outer prism velocity command MSByte	ϕ_{Out} outer motor direct command MSByte	Not used
5	Parallel Output Rate (bits 7-0)	θ position command LSByte	ϕ position command LSByte	V_{out} outer prism velocity command LSByte	ϕ_{Out} outer motor direct command LSByte	Not used
6	Message Checksum (Add bytes 0 through 5)					

Notes:

1. Parallel Port update rate LSB = 1Hz. Limits = [0..100KHz]. See Section 0 for parallel output description and formats.
2. [Ψ, θ] LSB = 31.95 *u*rads.
3. [ALT, ϕ] LSB = 95.87 *u*rads (Limit = +/-p).
4. [V_{in}, V_{out}] Velocity LSB = 1 rotation per minute (rpm).

Table 2-4 RPA Response Message Format

Byte #	**Description**					
0	Message Header Byte (0xCB)					
1	Mode Status: 000c ssss Where: c = checksum error ssss = mode command echo:					
	0x0 = Parallel port status[1]	0x1 = [Ψ, θ] system pointing angle status[2]	0x2 = [ALT, ϕ] system pointing angle status[3]	0x3 = [V_{in}, V_{out}] prism velocity status[4]	0x4 = [ϕ_{In}, ϕ_{Out}] motor angular position status[5]	0xC – 0xF = Requested system status response[6] C= [Ψ, ?] D= [ALT, ϕ] E=[V_{in},V_{out}] F= [ϕ_{In}, ϕ_{Out}]
2	Parallel Port Mode Status: 0= [Ψ, θ] 1= [ALT, ϕ] 2= [ϕ_{In}, ϕ_{Out}]	Ψ position status MSByte	ALT position status MSByte	V_{in} inner prism velocity status MSByte	ϕ_{In} inner motor direct status MSByte	w1 requested status MSByte
3	Parallel Output Rate status (bits 11-8)	Ψ position status LSByte	ALT position status LSByte	V_{in} inner prism velocity status LSByte	ϕ_{In} inner motor direct status LSByte	w1 requested status LSByte
4	Parallel Output Rate status (bits 7-4)	θ position status MSByte	ϕ position status MSByte	V_{out} outer prism velocity status MSByte	ϕ_{Out} outer motor direct status MSByte	w2 requested status MSByte
5	Parallel Output Rate status (bits 3-0)	θ position status LSByte	ϕ position status LSByte	V_{out} outer prism velocity status LSByte	ϕ_{Out} outer motor direct status LSByte	w2 requested status LSByte
6	Message Checksum (Addition of bytes 0 through 5)					

Notes:

1. Parallel Port Update Rate status LSB=1Hz.
2. [Ψ, θ] LSB = 31.95 *u*rads
3. [ALT, ϕ] LSB = 95.87 *u*rads.
4. [V_{in}, V_{out}] Velocity LSB = 1 rotation per minute (rpm).
5. [ϕ_{In}, ϕ_{Out}] Direct motor commands LSB = 95.87 *u*rads

2.1.2 Parallel Port

The Parallel Port is responsible for continuous output of the user-requested system pointing angles. The details of this interface are described in Table 2-5. This implementation of this port is part of Connector JP3 (see section 3.0).

Table 2-5 Parallel Port Interface Details

Protocol :		Single ended LVTTL signals				
Rate :		User selectable via Command Port up to 100 KHz				
Name	**Description**	**Source**	**Dest.**	**Addr Offset**	**Units**	**Limit/Range**
Valid when Parallel Port Mode = 0 (Ψ, θ), set via Command Port :						
Pout1	Current Ψ state	Support Electronics	User	0x6	LSB=31.95 urads	16 bits data word
Pout2	Current θ state	Support Electronics	User	0x7	LSB=31.95 urads	16 bits data word
Valid when Parallel Port Mode = 1 (ALT, ϕ), set via Command Port:						
Pout1	Current Alt state	Support Electronics	User	0x6	LSB=95.87 urads	16 bits data word
Pout2	Current ϕ state	Support Electronics	User	0x7	LSB=95.87 urads	16 bits data word
Valid when Parallel Port Mode = 2 (ϕ_{In}, ϕ_{Out}) , set via Command Port:						
Pout1	Current ϕ_{In} state	Support Electronics	User	0x6	LSB=95.87 urads	16 bits data word
Pout2	Current ϕ_{Out} state	Support Electronics	User	0x7	LSB=95.87 urads	16 bits data word

Data output is in a serial/parallel format. Four 8 bit words will be transmitted every 10 microseconds, along with a clock to indicate when the data words are valid. Figure 2-2 shows a timing diagram of the output data. The outputs will be single ended LVTTL level signals. Set up and hold times will be approximately 100 nanoseconds.

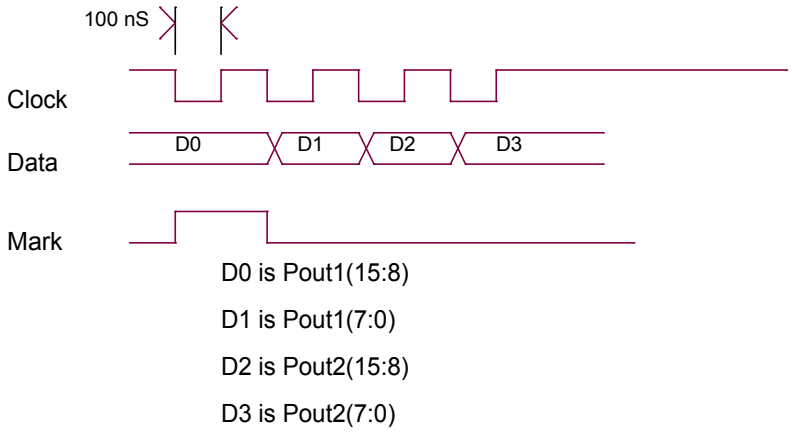

Figure 2-2 Parallel output timing diagram

3.0 CONNECTORS DESCRIPTIONS

3.1 JP3

Table 3-1. JP3 Connector Description

JP3 User Interface			26 pin header 0.1 inch centers 3M 2526-6002UB or equivalent.
Pin Number	**Name**	**I/O**	**Description**
1	DOUT7	OUTPUT	Parallel word MSB
2	DOUT6	OUTPUT	Parallel word
3	DOUT5	OUTPUT	Parallel word
4	DOUT4	OUTPUT	Parallel word
5	DOUT3	OUTPUT	Parallel word
6	DOUT2	OUTPUT	Parallel word
7	DOUT1	OUTPUT	Parallel word
8	DOUT0	OUTPUT	Parallel word LSB
9	TC	OUTPUT	Parallel word mark pulse. See Figure 2-2
10	CLKO	OUTPUT	Parallel clock. See Figure 2-2
11	VCCEXT	INPUT	Voltage for TTL serial port. 5 volts maximum.
12	+15V	POWER	Power for user circuits. 100 mA maximum
13	LLRX	INPUT	User TTL serial port input. Voltage set by VCCEXT.
14	+15V	POWER	Power for user circuits. 100 mA maximum
15	LLTX	OUTPUT	User TTL serial port output. Voltage level set by VCCEXT.
16	-15V	POWER	Power for user circuits. 100 mA maximum
17	LLRXI	INPUT	User RS232 serial port input
18	-15V	POWER	Power for user circuits. 100 mA maximum
19	LLTXO	OUTPUT	User RS232 serial port output
20	GND	POWER	Return for +/- 15 V
21	NC		No connection
22	GND	POWER	Return for +/- 15V
23	NC		No connection
24	NC		No connection
25	NC		No connection
26	NC		No connection

3.2 J3

Table 3-2 J3 Connector Description

J3 Power Input		Molex 22-05-3061 Mating connector Molex 22-01-3067
Pin	**Name**	**Description**
1	+28V	28 +/- 2Vdc @ 6 amps maximum
2	+28V	28 +/- 2Vdc @ 6 amps maximum
3	28 VRTN	28 volt return
4	28 VRTN	28 volt return
5	Chassis GND	Chassis ground
6	Chassis GND	Chassis ground

3.3 JP5

Table 3-3 JP5 Connector Description

JP5 Factory test			10 X 2 header 2 mm spacing FCI 98464
Pin Number	**Name**	**I/O**	**Description**
1	NC		no connect
2	M1ENABLE	OUTPUT	Logic 1 when axis 1 pwm amplifier enabled
3	NC		no connect
4	M2ENABLE	OUTPUT	Logic 1 when axis 2 pwm amplifier enabled
5	VCC3	POWER	3.3 volts for test fixture
6	LLTXO	OUTPUT	User RS232 interface
7	VA1	OUTPUT	Analog voltage; axis 1 PWM amplifier input
8	LLRXI	INPUT	User Rs232 interface
9	VA2	OUTPUT	Analog voltage; axis 2 PWM amplifier input
10	AXIS1A	OUTPUT	Axis 1 encoder AQB (LVTTL)
11	VB1	OUTPUT	Analog voltage; axis 1 PWM amplifier input
12	AXIS1B	OUTPUT	Axis 1 encoder AQB (LVTTL)
13	VB2	OUTPUT	Analog voltage; axis 2 PWM amplifier input
14	AXIS1IND	OUTPUT	Axis 1 encoder index pulse (LVTTL)
15	DGND	POWER	3.3 volt return
16	AXIS2A	OUTPUT	Axis 2 encoder AQB (LVTTL)
17	DGND	POWER	3.3 volt return
18	AXIS2B	OUTPUT	Axis 2 encoder AQB (LVTTL)
19	DGND	POWER	3.3 volt return
20	AXIS2IND	OUTPUT	Axis 2 encoder index pulse (LVTTL)

3.4 JP4

Table 3-4 JP4 Connector Description

JP4			10 X 2 header 2 mm spacing
Factory test			FCI 98464
Pin Number	Name	I/O	Description
1	TMS		DSP JTAG INTERFACE
2	TRSTN		DSP JTAG INTERFACE
3	TDI		DSP JTAG INTERFACE
4	EMU1		DSP JTAG INTERFACE
5	VCC3	POWER	3.3 VOLTS FOR TEST FIXTURE
6	PMDTXO	OUTPUT	PMD RS232 INTERFACE
7	TDO		DSP JTAG INTERFACE
8	PMDRXI	INPUT	PMD RS232 INTERFACE
9	TCK		DSP JTAG INTERFACE
10	TDI1		FPGA JTAG INTERFACE
11	TCK		DSP JTAG INTERFACE
12	TDO2		FPGA JTAG INTERFACE
13	TMS1		FPGA JTAG INTERFACE
14	TCK1		FPGA JTAG INTERFACE
15	DGND	POWER	3.3 VOLT RETURN
16	EMU0		DSP JTAG INTERFACE
17	REMAMPN	INPUT	LOGIC 0 ENABLES REMOTE PWM AMPLIFIER CONTROL
18	DGND	POWER	3.3 VOLT RETURN
19	REMDIS		LOGIC 0 ENABLES PWM AMPLIFIERS
20	DGND	POWER	3.3 VOLT RETURN

3.5 J2

Table 3-5 J2 Connector Description

J2 Optical Head			25 pin micro D connector Airborn MK263-025-445-220S
Pin Number	**Name**	**I/O**	**Description**
1	IND2-	INPUT	AXIS 2 ENCODER INDEX PULSE DIFFERENTIAL SIGNAL
2	QUADB2-	INPUT	AXIS 2 ENCODER AQB DIFFERENTIAL SIGNAL
3	QUADA2-	INPUT	AXIS 2 ENCODER AQB DIFFERENTIAL SIGNAL
4	VCC5	POWER	+5 VOLTS ENCODER POWER
5	DGND	POWER	5 VOLT RETURN
6	OBLACK	OUTPUT	AXIS 1 MOTOR DRIVE
7	ORED	OUTPUT	AXIS 1 MOTOR DRIVE
8	IWHITE	OUTPUT	AXIS 2 MOTOR DRIVE
9	DGND	POWER	5 VOLT RETURN
10	VCC5	POWER	+5 VOLTS ENCODER POWER
11	IND1+	INPUT	AXIS 1 ENCODER INDEX PULSE DIFFERENTIAL SIGNAL
12	QUADB1+	INPUT	AXIS 1 ENCODER AQB DIFFERENTIAL SIGNAL
13	QUADA1+	INPUT	AXIS 1 ENCODER AQB DIFFERENTIAL SIGNAL
14	IND2+	INPUT	AXIS 2 ENCODER INDEX PULSE DIFFERENTIAL SIGNAL
15	QUADB2+	INPUT	AXIS 2 ENCODER AQB DIFFERENTIAL SIGNAL
16	QUADA2+	INPUT	AXIS 2 ENCODER AQB DIFFERENTIAL SIGNAL
17	DGND	POWER	5 VOLT RETURN
18	CHASSIS GND	GND	
19	OWHITE	OUTPUT	AXIS 1 MOTOR DRIVE
20	IBLACK	OUTPUT	AXIS 2 MOTOR DRIVE
21	IRED	OUTPUT	AXIS 2 MOTOR DRIVE
22	DGND	POWER	5 VOLT RETURN
23	IND1-	INPUT	AXIS 1 ENCODER INDEX PULSE DIFFERENTIAL SIGNAL
24	QUADB1-	INPUT	AXIS 1 ENCODER AQB DIFFERENTIAL SIGNAL
25	QUADA1-	INPUT	AXIS 1 ENCODER AQB DIFFERENTIAL SIGNAL

3.6 Jumper J1

Table 3-6 Jump J1 configuration options

Pin Connections	Command Port Configuration
1-2	RS232
2-3	LVTTL

4.0 MECHANICAL LAYOUT

The details of the mechanical interface are described in Figure 4-1.

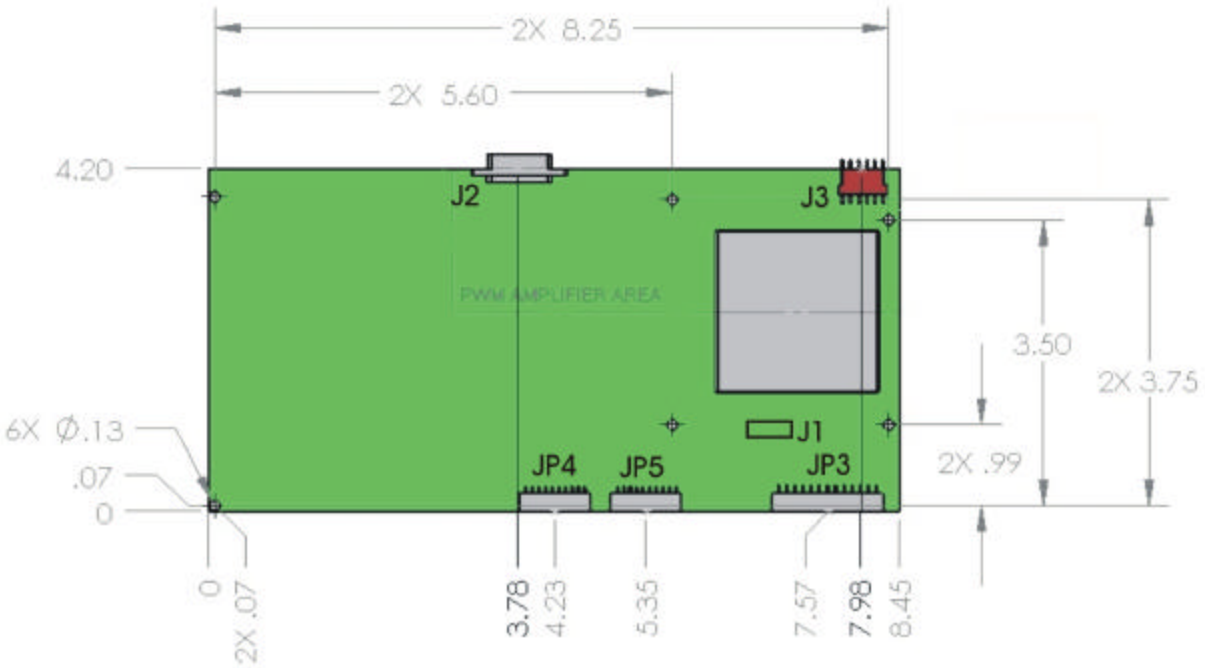

Figure 4-1 RPA Controller Board Dimensions

5.0 ACROYNMS/GLOSSARY

Table 5-1. Table Of Acroynms

ALT	Altitude
bps	Bits per second
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
LVTTL	Low Voltage TTL
ICD	Interface Control Document
I/O	Input/Output
PMD	Performance Motion Devices
RPA	Risley Prism Assembly
rpm	Rotations per minute
RS232	Standard UART serial port
SCI	Serial Control Interface
SW	Software
XINT	External Interface